Fig. 1

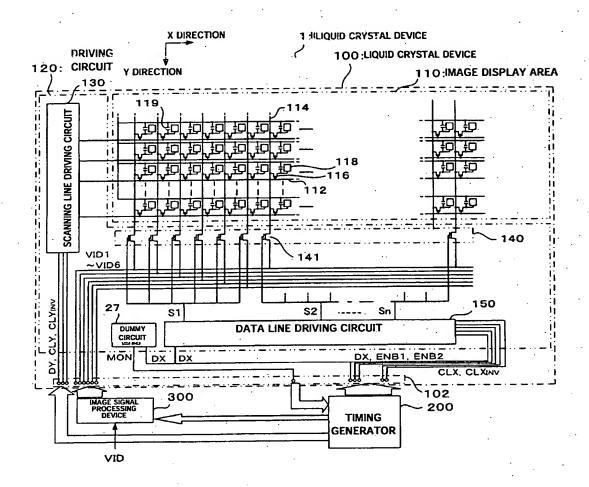


Fig. 2

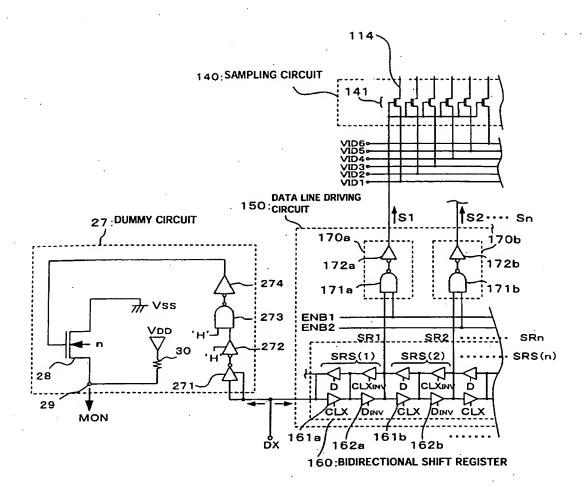


Fig. 3

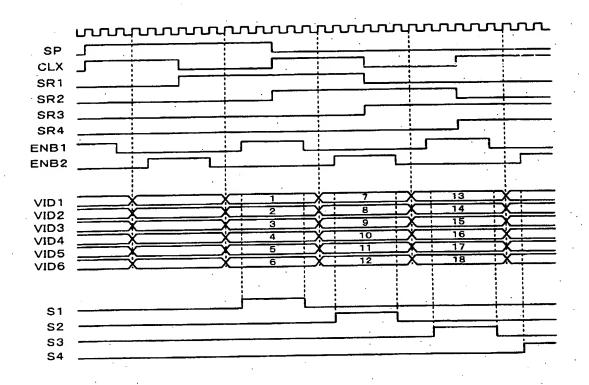


Fig. 4

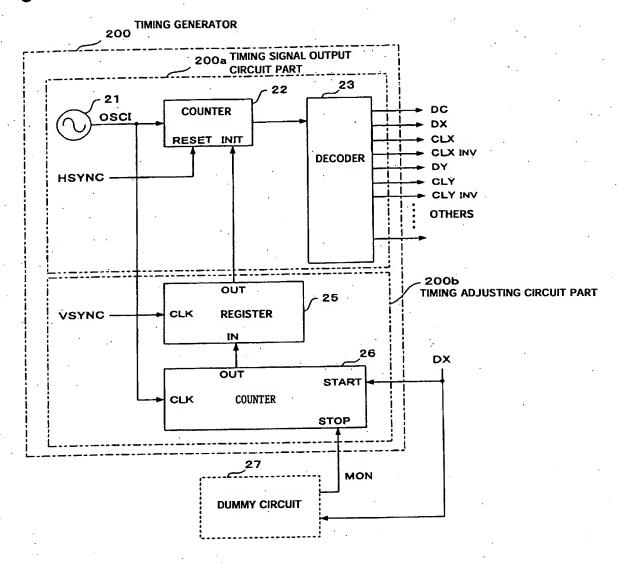
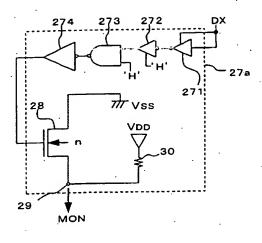


Fig. 5b



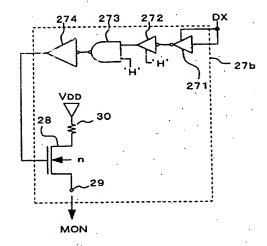


Fig. 5c

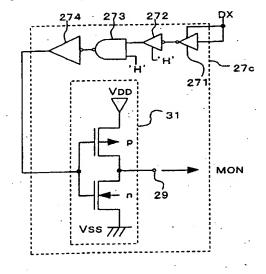


Fig. 6a

Fig. 6b

MON
DETECTION
SIGNAL OF
DUMMY CIRCUIT
27

VMON < VDD

VMON < VDD

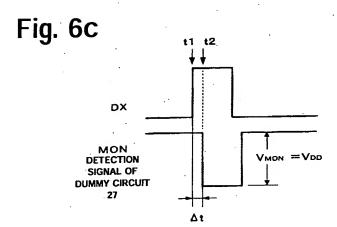


Fig. 7

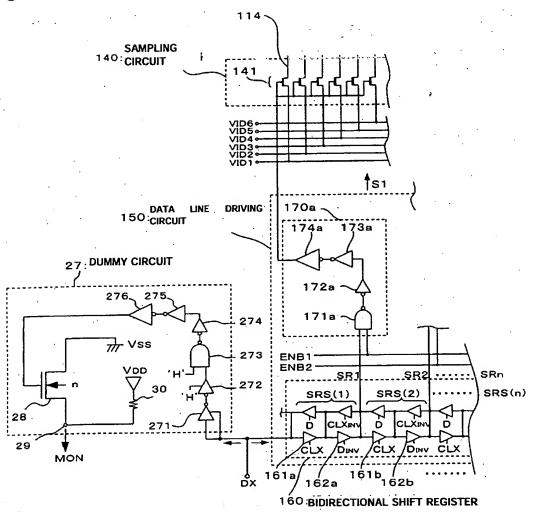


Fig. 8

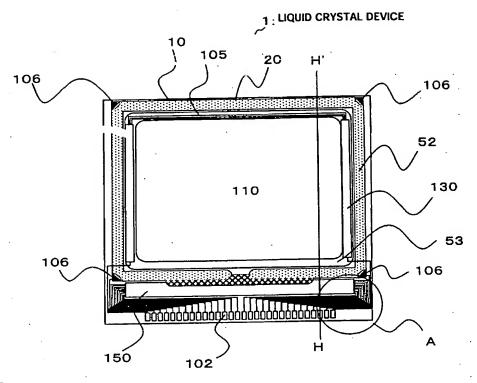


Fig. 9

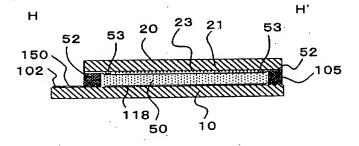


Fig. 10

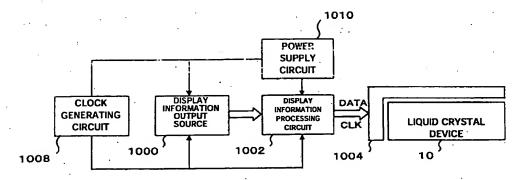


Fig. 11

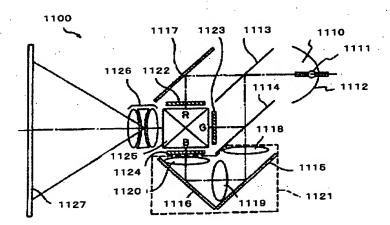


Fig. 12

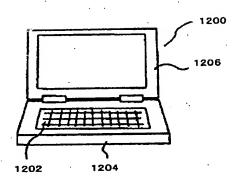


Fig. 13

